Emulation Board - 100

Emulation IC
104

Reconfigurable
Interconnect IC
106

To/From
Other
Emulation
Resources

112

Board Bus 108

On Board Trace
Memory
110

On-Board Data
Processing Resources
102

To/From
Control
Workstation

Figure 1

Emulation IC - 104

MEM
206

DBR
208

RLR
202

CTX
210

RIN
204

MSR
216

To/From
Other
Emulation
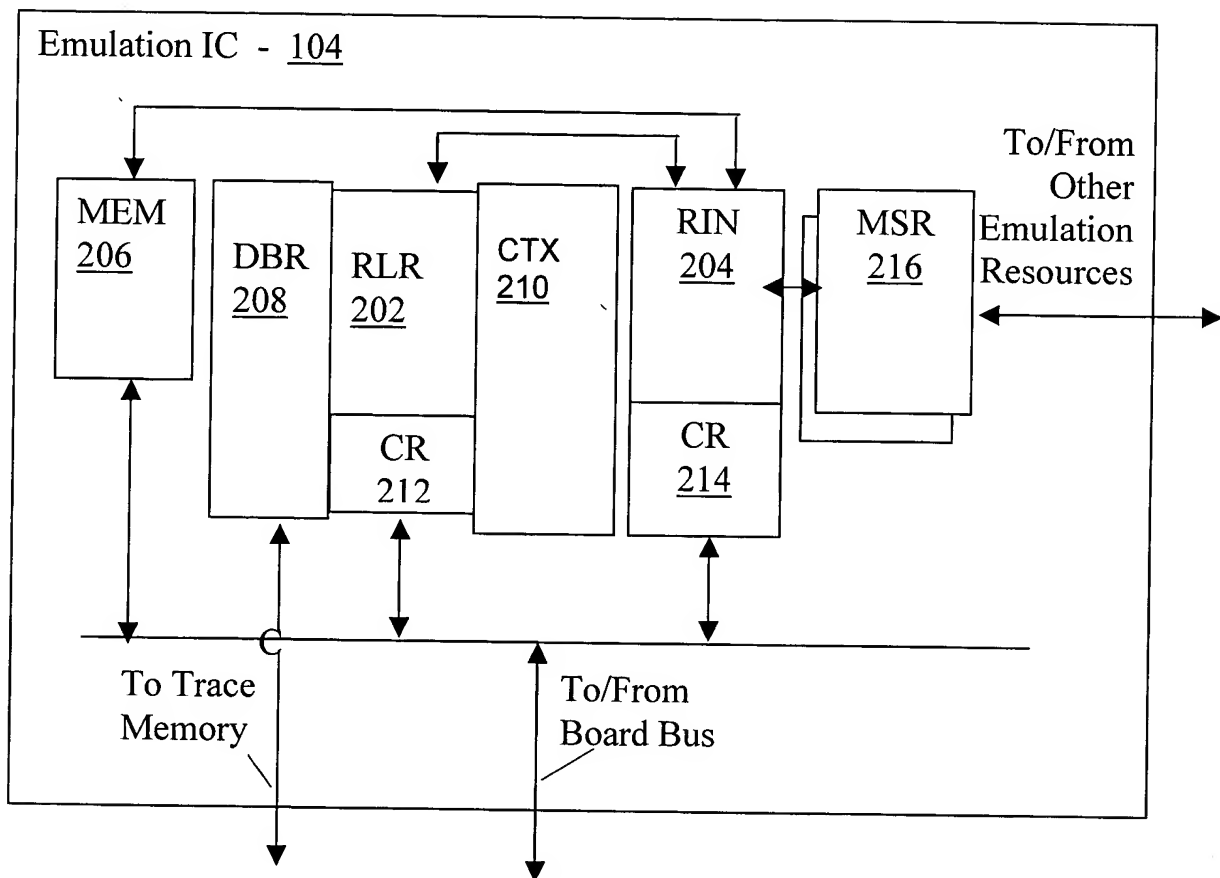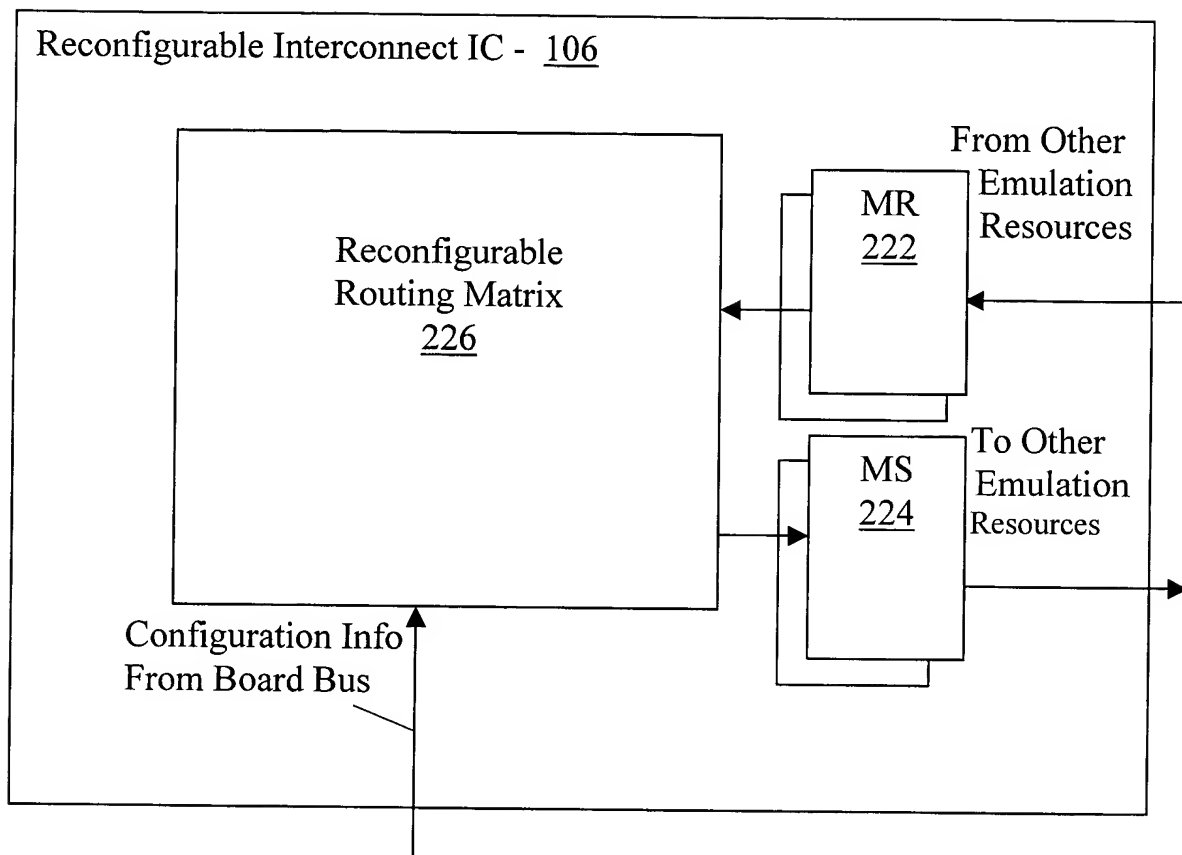Resources

CR
212

CR
214

To Trace
Memory

To/From
Board Bus

Key:
RLR = Reconfigurable Logic Resources
RIN = Reconfigurable Interconnect Network
MEM = Memory
DBR = Debugging Resources
CR = Configuration Registers
CTX = Context/State Element
MSR = Message Send and Receive

Figure 2a

Figure 2b

Op
Clock

Addr
Gen'r
328a

Storage [n bit
Schedule]
326a

316a

314b

314a

1

1

Parity Gen
312a

1

n - 1

224

318

316b

314c

314d

1

Parity Gen
312b

Compare 320

n-1

Bfr
322

n-1

Bfr
324

n-1

Op
Clock

Addr
Gen'r
328b

Storage [n bit
Schedule]
326b

222

Message Send & Receive 216
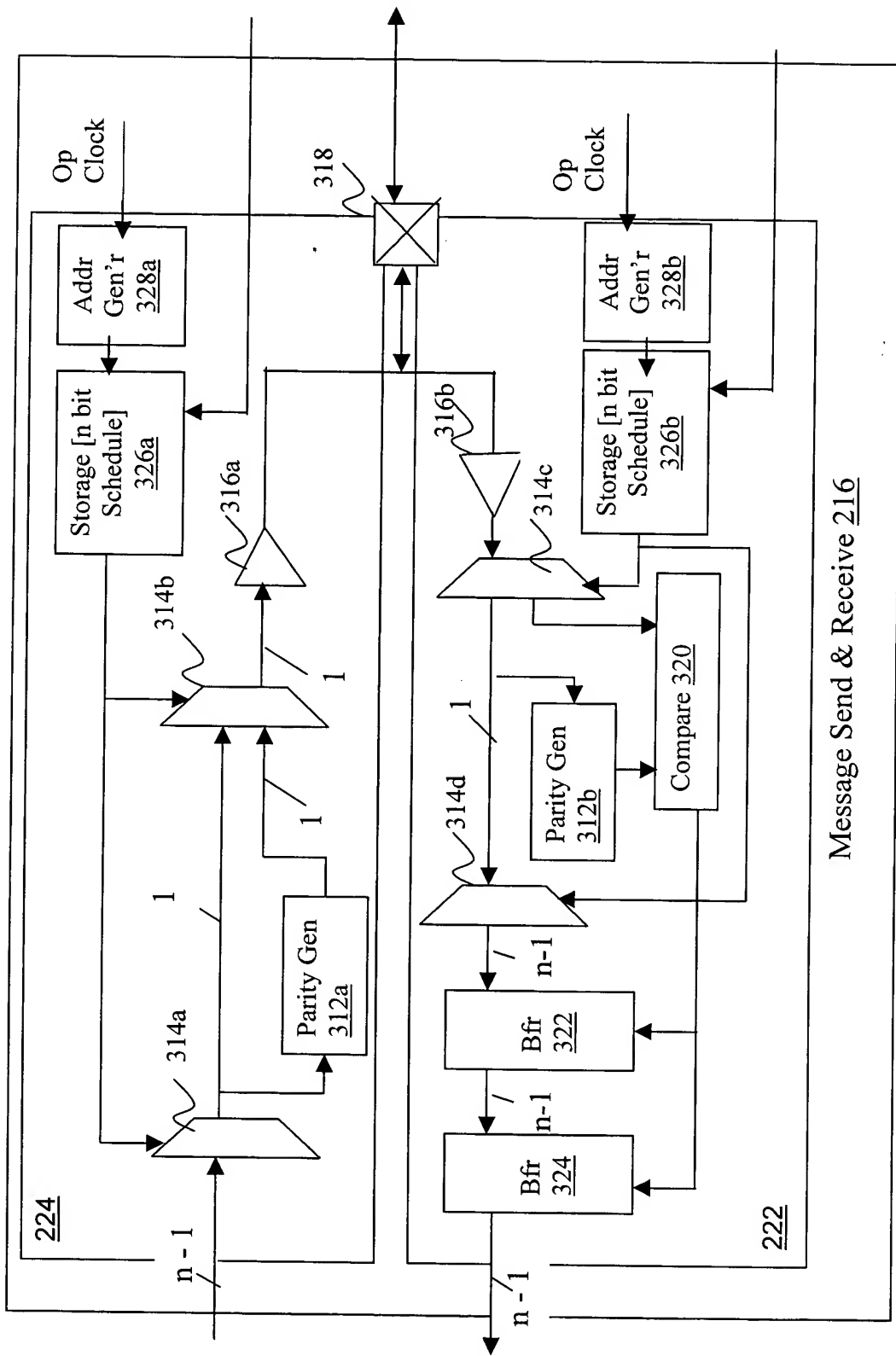
Figure 3

A
B
A
C
A
B
A
D
A
B
A
C
A
B
A
parity value

Figure 4

Control Workstation 502

Design Circuit
Mapping Software
504

Emulator 506

Emulation Boards 100

Reconfig
Interconnect 106

Emulation
ICs 104

Service and
I/O Boards
508

Inter-Board Interconnect 510

Figure 5

A → B

More Emul
Board? 614

Done

Receive Circuit Design
to be emulated
602

Partition Circuit
Design and Map
Circuit Elements to
Emulation Boards 604

Partition Circuit Elements
Assigned to an Em Board and
Map Circuit Elements to Em.
ICs 606

Partition Circuit Elements
Assigned to an EM. IC and Map
Circuit Elements to RLR,
Interconnect RLR, including
development of Signal Messaging
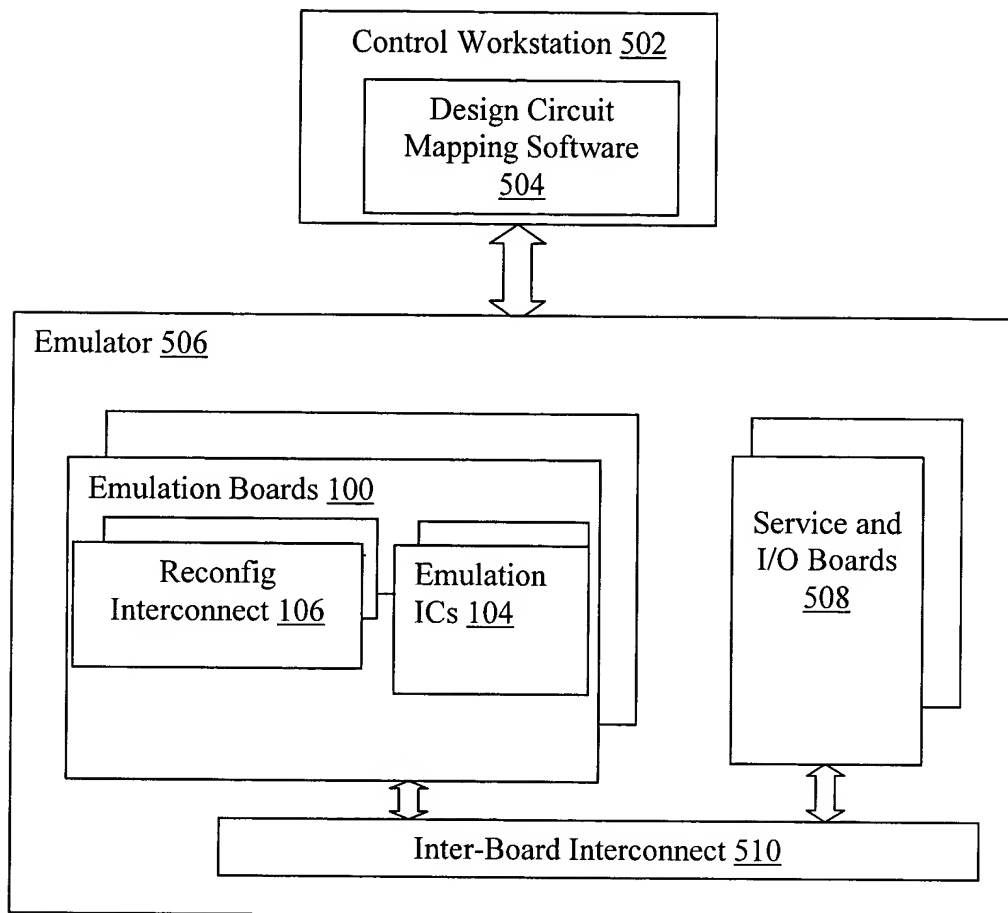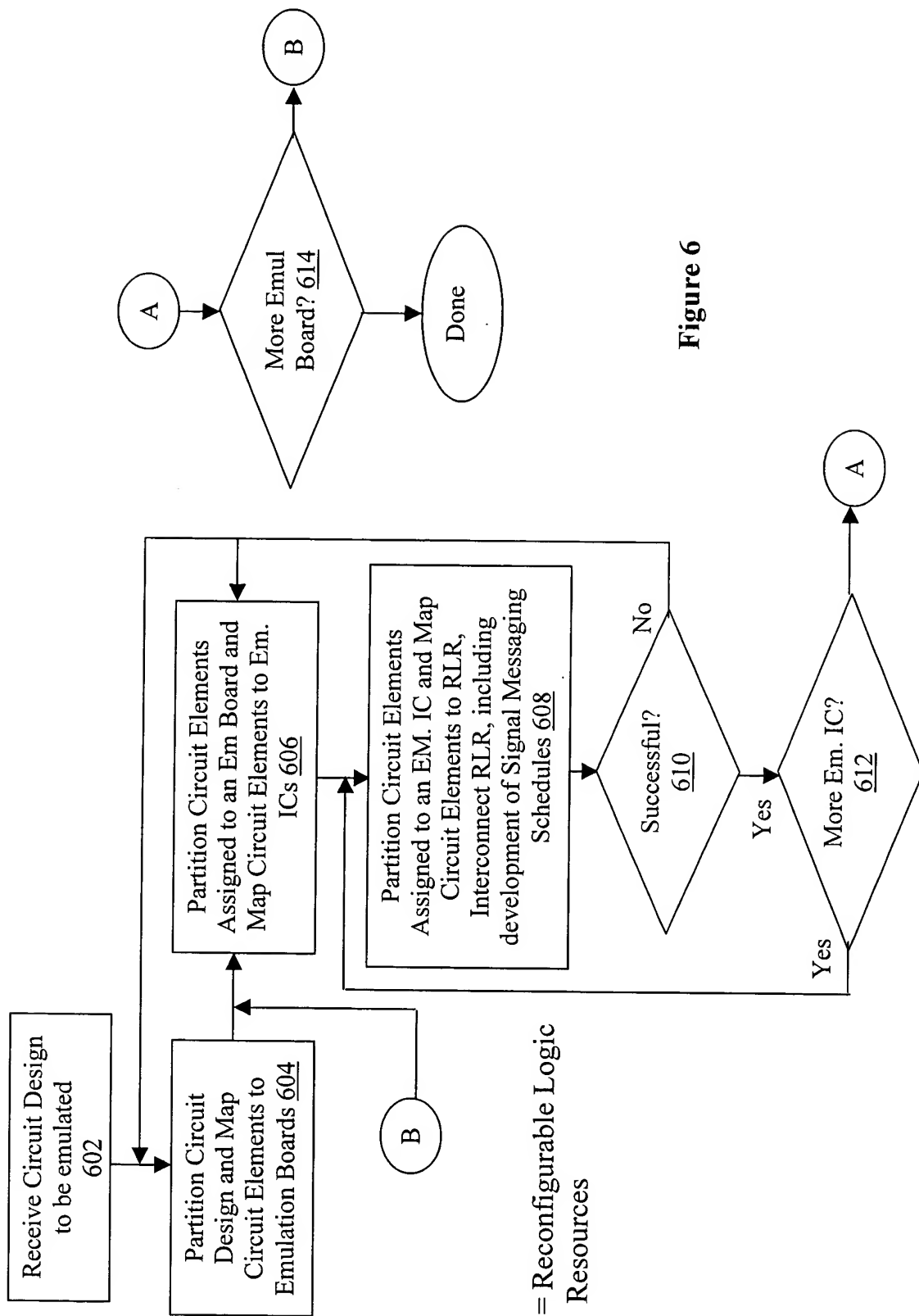Schedules 608

Successful?
610

No

Yes

More Em. IC?
612

Yes

A

B

Key:
RLR = Reconfigurable Logic
Resources

Figure 6

For each signal of an emulation IC that needs to be transferred to another emulation IC determine a time criticalness of the signal
702

For each signal of the emulation IC, determine an inclusion frequency based on the determined time criticalness of the signal
704

Group signals by their determined inclusion frequencies to generate messaging schedules for the various message send/receive blocks of the emulation IC 706

Figure 7